

Abstract of the Disclosure

The preferred embodiments described herein provide a memory device and method for selectable sub-array activation. In one preferred embodiment, a memory array is provided comprising a plurality of groups of sub-arrays and circuitry operative to simultaneously write data into and/or read data from a selected number of groups of sub-arrays. By selecting the number of groups of sub-arrays into which data is written and/or from which data is read, the write and/or read data rate is varied. Such varying can be used to prevent thermal run-away of the memory array. Other preferred embodiments are provided, and each of the preferred embodiments can be used alone or in combination with one another.

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